Midterm Review Solutions

CS 465- Fall 2021

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Questions

- What is CPI?

- Suppose that 15% of the instructions of a program take 2 cycles, 25% take 3 cycles, and 60% take 1 cycle. What is the CPI of the program?

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  - A: cycles per instruction

- Suppose that 15% of the instructions of a program take 2 cycles, 25% take 3 cycles, and 60% take 1 cycle. What is the CPI of the program?
  - A: 0.15*2 + 0.25*3+0.6*1 = 1.65

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- Suppose the same program above executes 1,000,000 instructions. How many cycles would it take to execute the program?
  - 1,000,000 * 1.65 = 1,650,000 cycles

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1,650,000 cycles * 200 * 10^{-12} = 3.3 * 10^{-4} sec = 0.33 msec

Question

- Suppose that compiler optimization is used to compile the same program as before. The optimization reduces the total number of instructions by 10% and now 12% of the instructions of the program take 2 cycles, 28% take 3 cycles, and 60% take 1 cycle. What is the execution time of the program now?

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$0.9 * 1{,}000{,}000 * (0.12 * 2 + 0.28 * 3 + 0.6 * 1) * 200 * 10^{-12} = 3.024 * 10^{-4}$ sec

Question

- Consider that 20% percent of a program's instructions are branch instructions and that the CPI for these instructions is 2. The CPI for the remaining instructions is 1.8. What would be the CPI of the program if the hardware designers improved the branch prediction algorithm so that the CPI of branch instructions went down to 1.2?

Question

- Consider that 20% percent of a program's instructions are branch instructions and that the CPI for these instructions is 2. The CPI for the remaining instructions is 1.8. What would be the CPI of the program if the hardware designers improved the branch prediction algorithm so that the CPI of branch instructions went down to 1.2?
  - 0.2 * 1.2 + 0.8 * 1.8 = 1.68

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  - The algorithm
  - Its input data
  - The language in which it is written
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Answer: all

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CPU time = # instructions * CPI * clock cycle duration

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The power wall. Processors are using too much power and dissipating too much heat at current clock frequencies

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No. MIPS only operates on registers.

Question

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- lw $t0, 8 ($s0)

Questions

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2's complement

Questions

- What is the sign bit of negative integer numbers in 2's complement?

- 1

- How do you negate a number?

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- How do you negate a number?

- Flip the bits and add 1

Question

- How would you compile the statement into MIPS using 3 instructions?

```
if (i==j) f = g;
else f = h;
```

where i, j, are in $t0, $t1, f, g, and h are stored in $s0, $s1, and $s2.

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where i, j, are in $t0, $t1, f, g, and h are stored in $s0, $s1, and $s2.

```
        add     $s0, $zero, $s1     # f = g
        beq     $t0,$t1,LABEL       # skip else if  i = j
ELSE    add     $s0, $zero, $s2     # f = h
LABEL   -------
```

Question

Consider the instructions

```
    slt $t0, $s1, $s2
    bne $t0, $zero, L1
L2  ……
    ……
L1
```

And consider that $s1 = 3 and $s2 = 5. What is the address branched to by the bne instruction?

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L2    ……
      ……
L1
```

And consider that $s1 = 3 and $s2 = 5. What is the address branched to by the bne instruction?

$t0 is set to 1. Then, branch to L1.

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```
jal Label
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It saves the address of the instruction following the jal in the $ra register and changes the PC to the address of the instruction that corresponds to Label

Question

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  jr $ra

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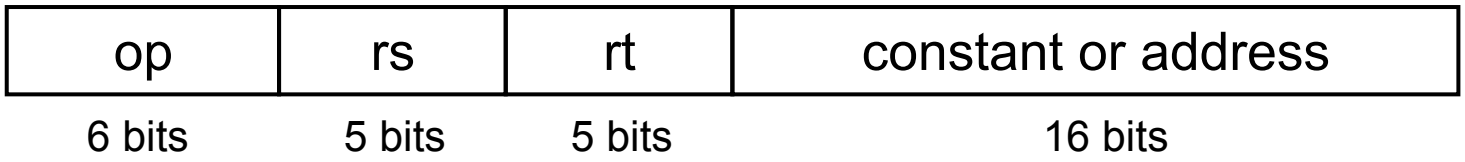
  jr $ra

It jumps to the address stored in the register $ra

Question

- Consider the beq instruction stored at address 1000_{10}. The value of the address field is 200_{10}. What is the address of the next instruction if rs and rt are equal?



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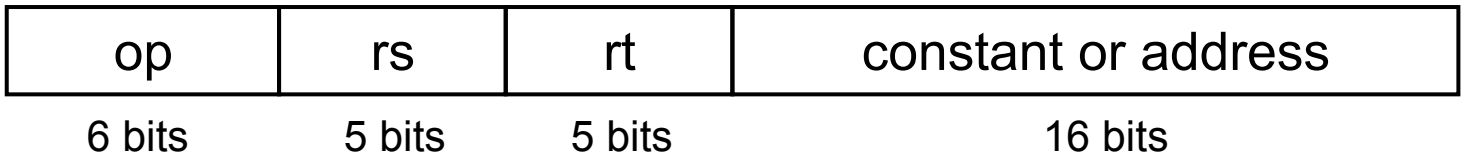
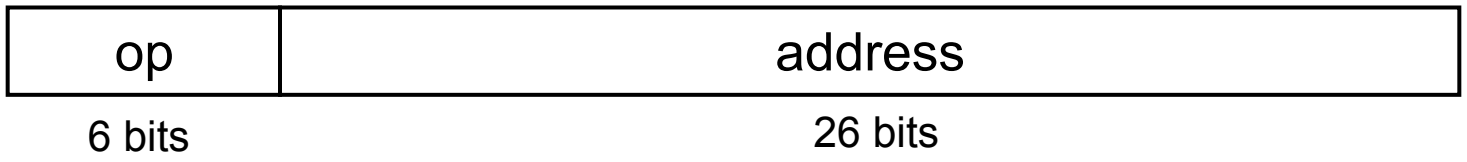


- If rs=rt, the target address of the branch is $(1000+4) + 200*4 = 1804_{10}$

Question

- Consider the jump instruction stored at address $A80094_{16}$. The value of the address field is 800_{10}. What is address in binary of the next instruction to be executed?



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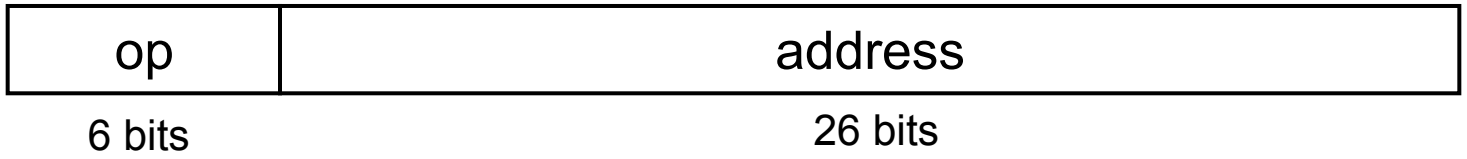

$A8009004_{16} + 4_{10} = A8009008_{16}$

=> A = 1010_2; $800*4=3200_{10}$ = 000 …110010000000_2

Target address = 1010: 800*4 =>1010000 …110010000000_2

Question

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- $100_{10} = 01100100_2 \Rightarrow -100_{10} = 10011100_2$
- $64_{10} = 01000000_2 \Rightarrow -64_{10} = 11000000_2$
- $-100-64 = 01011100_2$

- Adding two negative numbers results in a positive number => overflow

Question

Consider a 2 x 3 matrix stored in memory in *column major order*, i.e., elements are stored column by column. Each element is 4-bytes long. What is the byte offset of element i,j?

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Byte offset of [i,j] =[j * 2 + i] * 4 because before [i,j] there are j full columns and i elements

Question

Write a minimal set of MIPS assembly instructions that does the identical operation as the C code below. Assume the base address of C is in $s1 and that A is in $s2. Use the minimum number of registers. Do not destroy the contents of $s1 or $s2.

A = C[0] << 4;

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A = C[0] << 4;

```
lw      $t1, 0($s1)     # $t1 <- C[0]
sll     $t1, $t1,4      # $t1 <- $t1 << 4
sw      $t1, 0($s2)     # A <- $t1
```

Exercise 2.26.1

Consider the following MIPS code with the following initial values: $t1 = 10 and $s2 = 0.

```
LOOP: slt    $t2, $0, $t1
      beq    $t2, $0, DONE
      subi   $t1, $t1, 1
      addi   $s2, $s2, 2
      j      LOOP
DONE:
```

What is the final value of $s2?

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      beq   $t2, $0, DONE
      subi  $t1, $t1, 1
      addi  $s2, $s2, 2
      j     LOOP
DONE:
```

What is the final value of $s2?

Number of loop executions:

$t1 at top = 10; $t1 at bottom = 9

…

t1 at top = 1; $t1 at bottom = 0 → 10 executions →$s2 = 2x10 = **20**

Question

Describe what the following MIPS code does.

```
        addi    $s2,$0,$0
        addi    $t1,$0,$0
LOOP    lw      $s1,0($s0)
        add     $s2,$s2,$s1
        addi    $s0,$s0,4
        addi    $t1,$t1,1
        slti    $t2,$t1,100
        bne     $t2,$0,LOOP
DONE:
```

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LOOP    lw      $s1,0($s0)
        add     $s2,$s2,$s1
        addi    $s0,$s0,4
        addi    $t1,$t1,1
        slti    $t2,$t1,100
        bne     $t2,$0,LOOP
DONE:
```

Code meaning: store in $s2 the sum of all 100 words stored starting at address $s0

Question

Consider a multiprocessor with p processors. Assume that 25% of the instructions of a program can be executed in parallel using all p processors. The remaining 75% of the instructions have to be executed sequentially. Assume that the time to execute the program sequentially (i.e., using only one processor) is Ts. Give an expression for S(p), the speedup obtained when using p processors.

What is the maximum possible speedup? i.e.(lim S(p) when p -> ∞)

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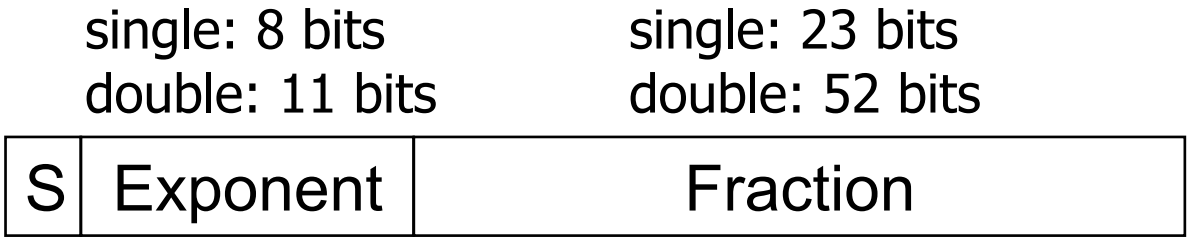
What is the maximum possible speedup? i.e.(lim S(p) when p -> ∞)

S(p) = Ts / (0.75 Ts + 0.25 Ts/p) = 1 / (0.75 + 0.25/p)

lim S(p) when p -> ∞ = 1 / 0.75 = 4/3 = 1.33

Floating Point



Single: Bias = 127; Double: Bias = 1023

What is the value of the exponent field and the fraction for the single precision representation of 1.75?

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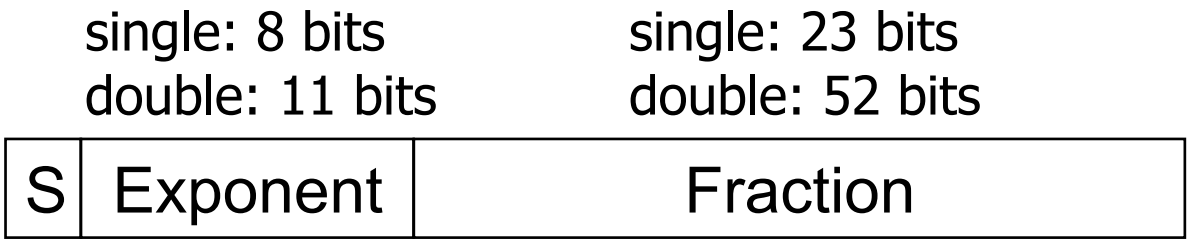

Single: Bias = 127; Double: Bias = 1023

What is the value of the exponent field and the fraction for the single precision representation of 1.75?

1.75 = 1 + 0.75 = 1 + 0.5 + 0.25
Fraction= 1100000…000
Exponent = actual + bias = 0 + 127 = 127 = 01111111_2

The Processor

- What is a single cycle datapath?
- What is the duration of a cycle in a single-cycle datapath?
- How does a pipelined architecture differ from a single cycle datapath?
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The time needed to execute the longest stage

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Generate selector bits that control the various multiplexers and units of the processor.

- Discuss the inputs of the control unit

- Discuss some of the outputs of the control unit

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MemRead, MemWrite, RegWrite, Branch, ALUSrc, MemToReg

The Processor

- What are the phases of a MIPS pipeline?

Instr. Fetch, Instr Decode, Execute, Memory Access, WriteBack

- What is duration of each phase in cycles?

- Consider the following instruction sequence:

  add $t5, $t1, $t2

  add $t6, $t3, $t4

Is there a data hazard assuming no forwarding? If yes, by how many cycles?

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No data hazard

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- Consider the following instruction sequence:

  add $t3, $t1, $t2

  add $t6, $t3, $t5

Is there a data hazard assuming no forwarding? If yes, by how many cycles?

Yes by 2 cycles

- Consider the instruction sequence above:

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No. $t3 can be sent by the end of EX of the first add to the input of EX for the second add

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- Consider the following instruction sequence:

  lw $t3, 16($t3)

  add $t6, $t3, $t5

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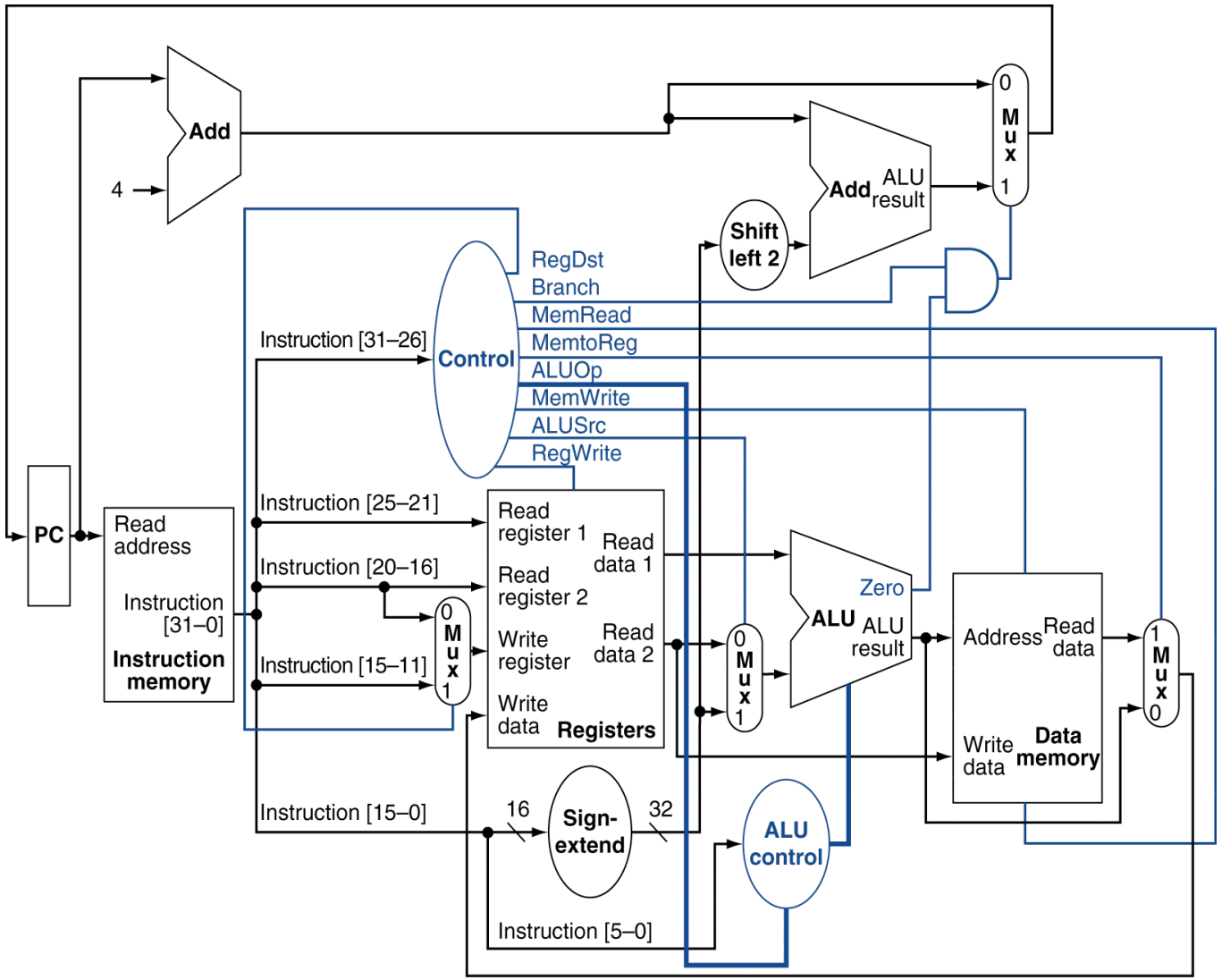
What is the value of RegDst for add $t1,$t2,$t3?

Hint: destination address in bits 15-11.



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Answer: 1

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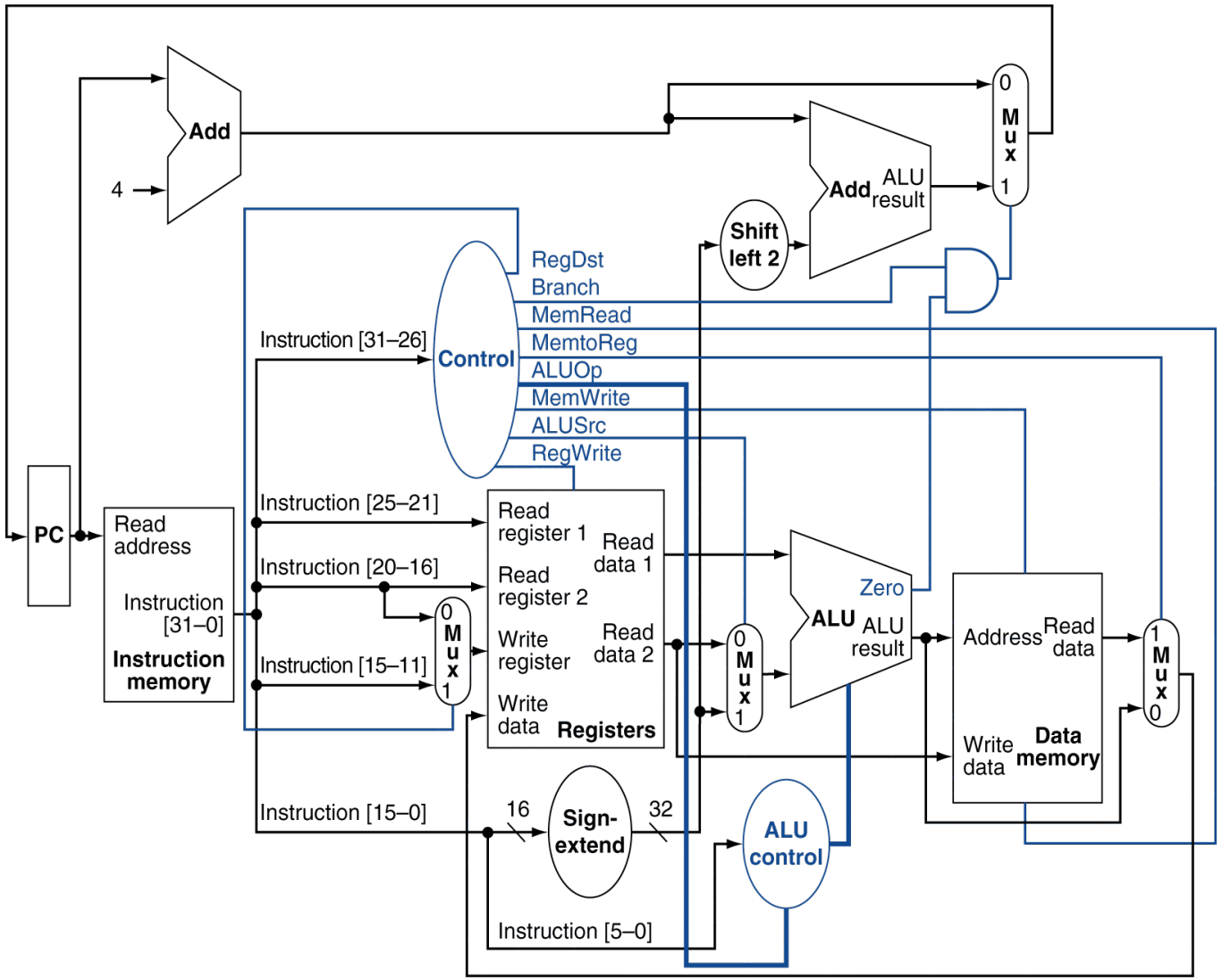
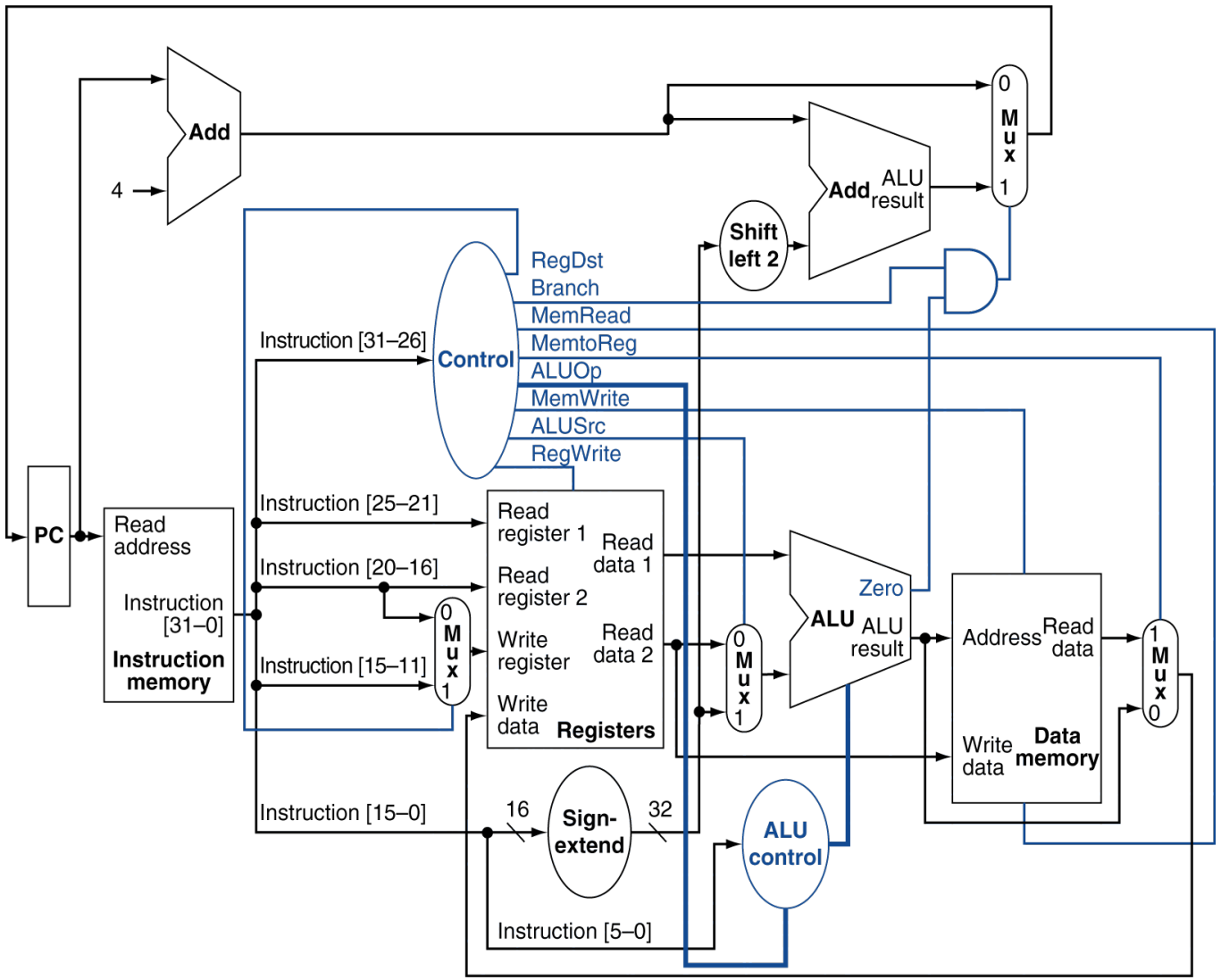


What is the value of ALUSrc for addi $t1,$t2,4?



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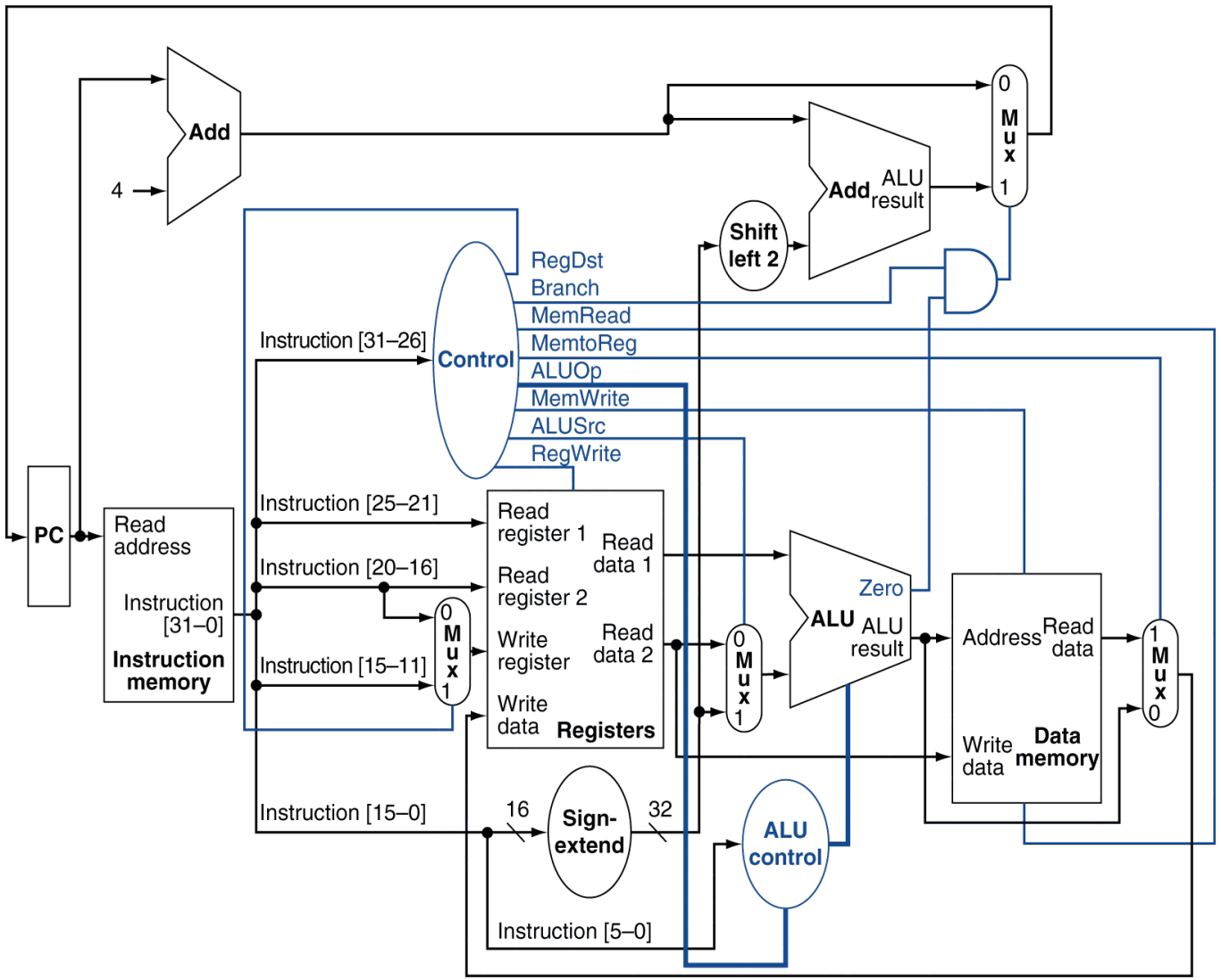
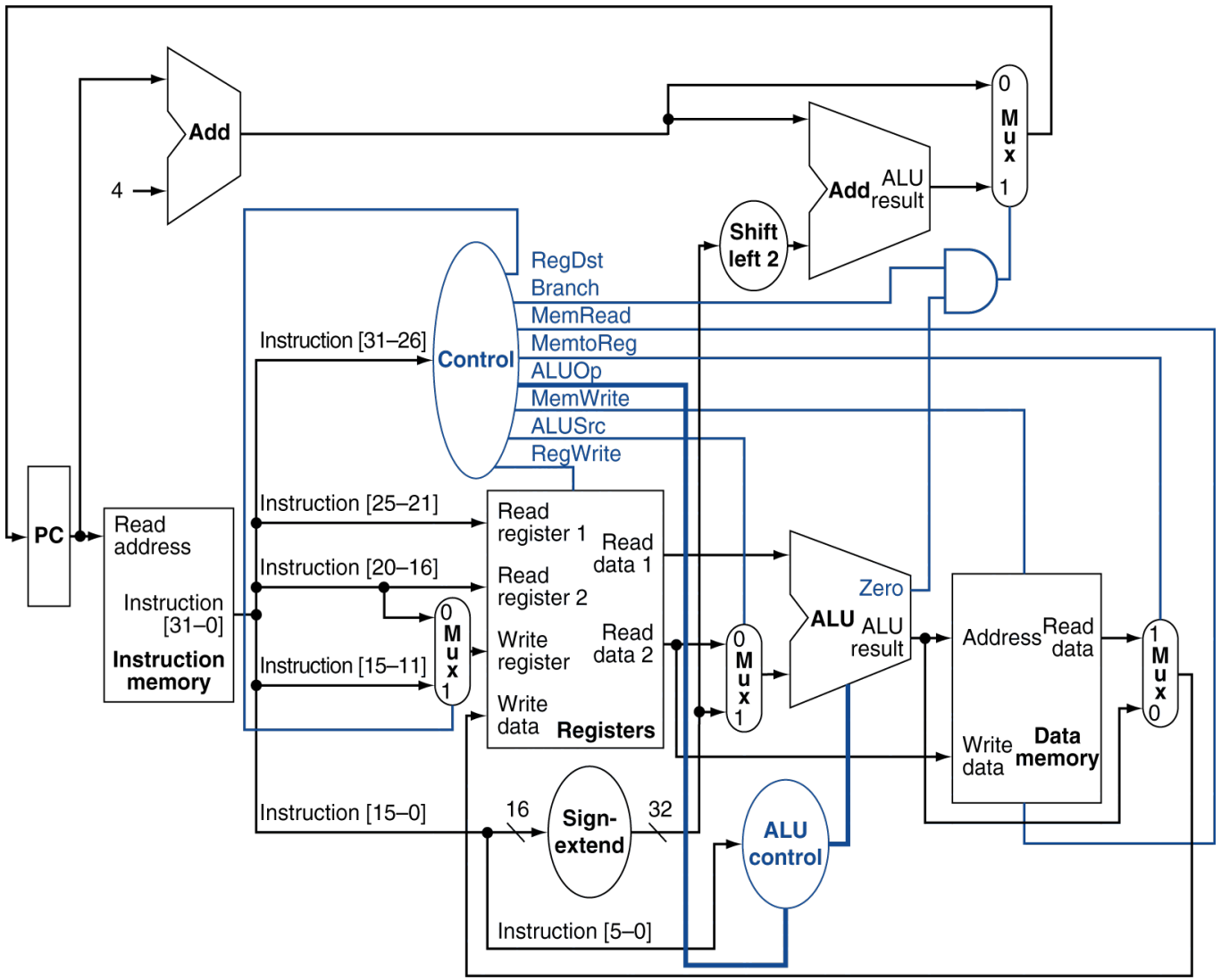
A: 1



What is the value of ALUSrc for lw $t2,4($t3)?



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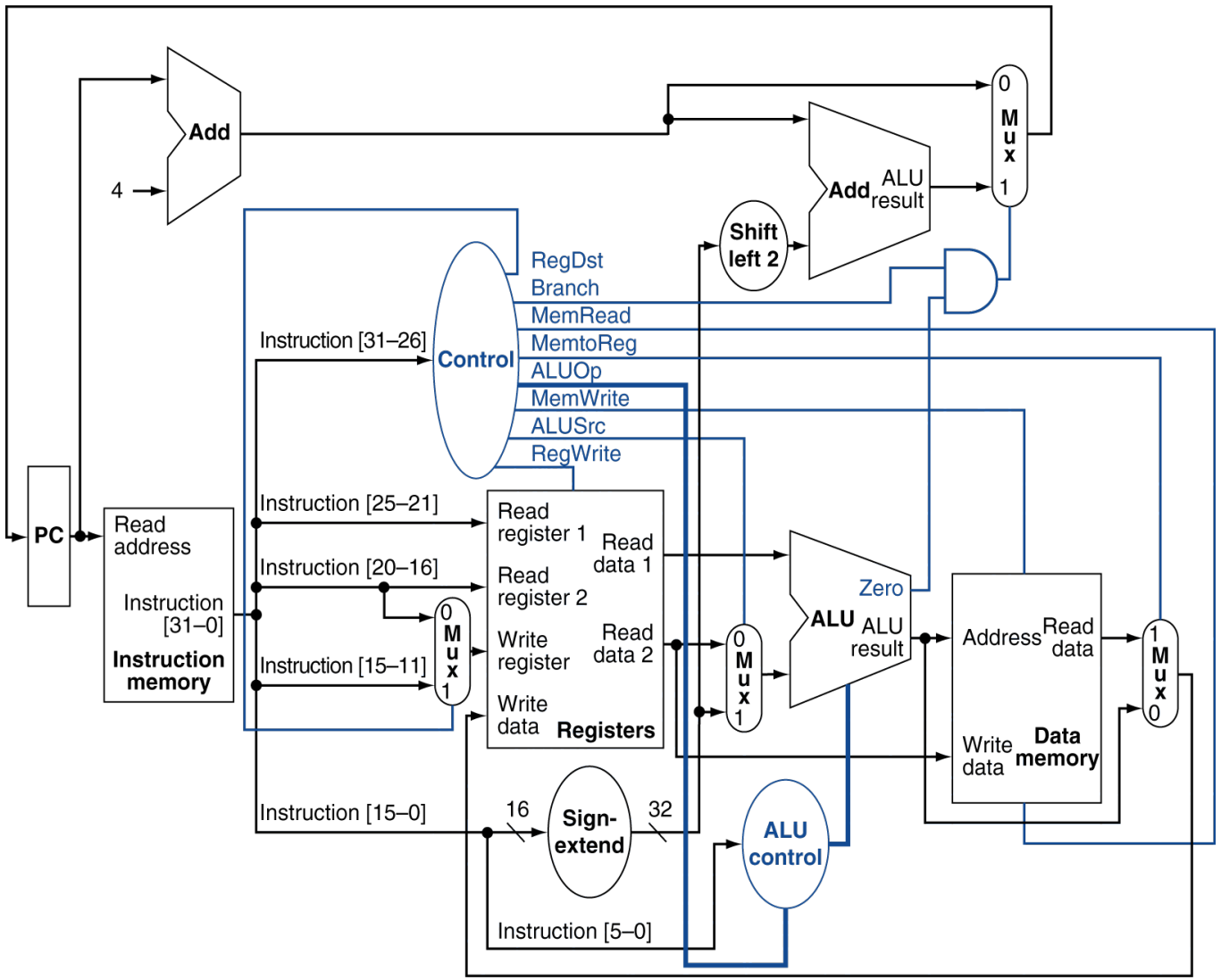

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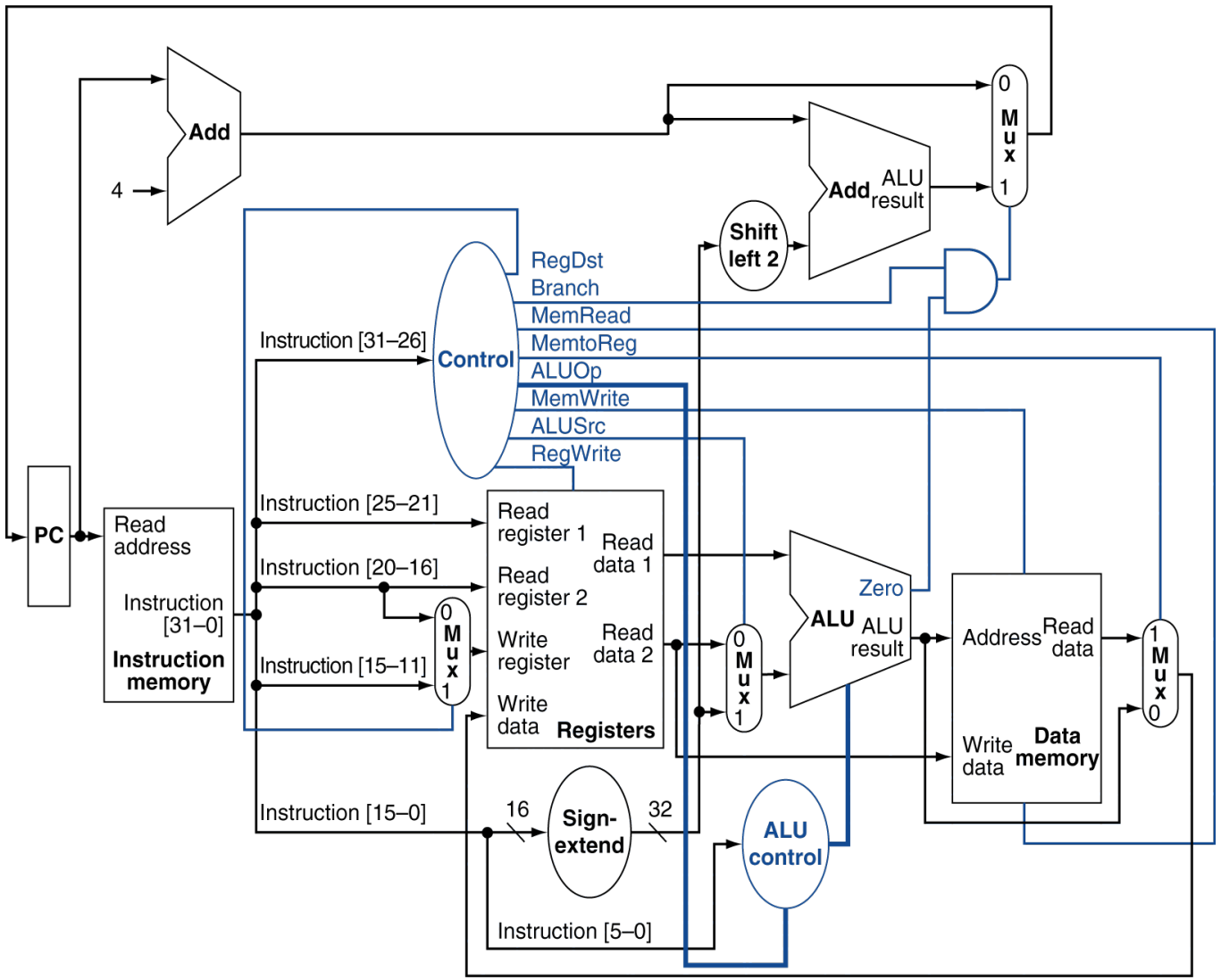

What is the value of ALUSrc for beq $t2,$t3,exit?

A: 0