

# Midterm Review

CS 465- Fall 2021

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# Questions

- What is CPI?
- Suppose that 15% of the instructions of a program take 2 cycles, 25% take 3 cycles, and 60% take 1 cycle. What is the CPI of the program?

# Question

- What is CPI?
- Suppose that 15% of the instructions of a program take 2 cycles, 25% take 3 cycles, and 60% take 1 cycle. What is the CPI of the program?
- Suppose the same program above executes 1,000,000 instructions. How many cycles would it take to execute the program?

# Question

- Suppose that the above program runs on a machine that has a cycle time of 200 ps. What is the execution time of the program on this machine?

# Question

- Suppose that compiler optimization is used to compile the same program as before. The optimization reduces the total number of instructions by 10% and now 12% of the instructions of the program take 2 cycles, 28% take 3 cycles, and 60% take 1 cycle. What is the execution time of the program now?

# Question

- Consider that 20% percent of a program's instructions are branch instructions and that the CPI for these instructions is 2. The CPI for the remaining instructions is 1.8. What would be the CPI of the program if the hardware designers improved the branch prediction algorithm so that the CPI of branch instructions went down to 1.2?

# Question

- Which of these elements can influence the number of instructions executed by a program?
  - The algorithm
  - Its input data
  - The language in which it is written
  - The compiler
  - The ISA

# Question

- How would you compute the CPU time of a program as a function of the number of instructions, the CPI, and the clock cycle duration?



# Question

- What is the motivation to design multicore computers?

# Question

- Is there any instruction in the MIPS ISA that allows a number in main memory to be added to a number in a register?

# Question

- What is the MIPS instruction needed to load element  $A[4]$  of array  $A$  into register  $\$t0$  assuming the address of the array is stored at register  $\$s0$  and that each element of the array is a 4-byte integer?

# Questions

- Why MIPS does not have a subtract immediate instruction?
- How are negative integer numbers represented in MIPS and in the majority of processors?

# Questions

- What is the sign bit of negative integer numbers in 2's complement?
- How do you negate a number?

# Question

- How would you compile the statement into MIPS using 3 instructions?

```
if (i==j) f = g;  
else f = h;
```

where i, j, are in \$t0, \$t1, f, g, and h are stored in \$s0, \$s1, and \$s2.

# Question

Consider the instructions

```
    slt $t0, $s1, $s2  
    bne $t0, $zero, L1
```

L2     .....

       .....

L1

And consider that  $\$s1 = 3$  and  $\$s2 = 5$ .  
What is the address branched to by the  
bne instruction?

# Question

- What is the purpose of the instruction below and what it does?

```
jal Label
```



# Question

- What is the purpose of the instruction below and what it does?

`jr $ra`

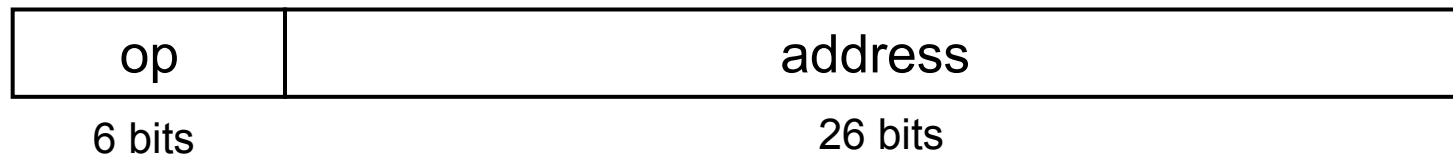
# Question

- Consider the beq instruction stored at address  $1000_{10}$ . The value of the address field is  $200_{10}$ . What is the address of the next instruction if rs and rt are equal?



# Question

- Consider the jump instruction stored at address  $A80094_{16}$ . The value of the address field is  $800_{10}$ . What is address in binary of the next instruction to be executed?



# Question

- Consider adding the numbers -100 and -64 represented in 2's complement using 8 bits. What is the result of the computation?

# Question

Consider a  $2 \times 3$  matrix stored in memory in *column major order*, i.e., elements are stored column by column. Each element is 4-bytes long. What is the byte offset of element  $i,j$ ?

# Question

Write a minimal set of MIPS assembly instructions that does the identical operation as the C code below. Assume the base address of C is in \$s1 and that A is in \$s2. Use the minimum number of registers. Do not destroy the contents of \$s1 or \$s2.

```
A = C[0] << 4;
```

# Exercise 2.26.1

Consider the following MIPS code with the following initial values:  
\$t1 = 10 and \$s2 = 0.

```
LOOP: slt  $t2, $0, $t1  
      beq  $t2, $0, DONE  
      subi $t1, $t1, 1  
      addi $s2, $s2, 2  
      j    LOOP
```

DONE:

What is the final value of \$s2?

# Question

Describe what the following MIPS code does.

```
        addi    $s2,$0,$0
        addi    $t1,$0,$0
LOOP    lw      $s1,0($s0)
        add     $s2,$s2,$s1
        addi   $s0,$s0,4
        addi   $t1,$t1,1
        slti   $t2,$t1,100
        bne    $t2,$0,LOOP
```

DONE:



# Question

Consider a multiprocessor with  $p$  processors. Assume that 25% of the instructions of a program can be executed in parallel using all  $p$  processors. The remaining 75% of the instructions have to be executed sequentially. Assume that the time to execute the program sequentially (i.e., using only one processor) is  $T_s$ . Give an expression for  $S(p)$ , the speedup obtained when using  $p$  processors.

What is the maximum possible speedup? i.e.  $(\lim_{p \rightarrow \infty} S(p))$

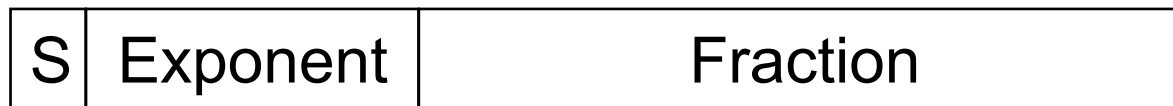
# Floating Point

single: 8 bits

double: 11 bits

single: 23 bits

double: 52 bits



Single: Bias = 127; Double: Bias = 1023

What is the value of the exponent field and the fraction for the single precision representation of 1.75?

# The Processor

- What is a single cycle datapath?
- What is the duration of a cycle in a single-cycle datapath?
- How does a pipelined architecture differ from a single cycle datapath?
- What is the duration of a cycle in a pipelined architecture?

# The Processor

- What is the purpose of the control unit?
- Discuss the inputs of the control unit
- Discuss some of the outputs of the control unit

# The Processor

- What are the phases of a MIPS pipeline?
- What is duration of each phase in cycles?
- Consider the following instruction sequence:  
    add \$t5, \$t1, \$t2  
    add \$t6, \$t3, \$t4

Is there a data hazard assuming no forwarding? If yes, by how many cycles?

# The Processor

- Consider the following instruction sequence:

add \$t3, \$t1, \$t2

add \$t6, \$t3, \$t5

Is there a data hazard assuming no forwarding? If yes, by how many cycles?

- Consider the instruction sequence above:

Is there a data hazard assuming forwarding is used? If yes, by how many cycles?

# The Processor

- Consider the following instruction sequence:

```
lw $t3, 16($t3)
```

```
add $t6, $t3, $t5
```

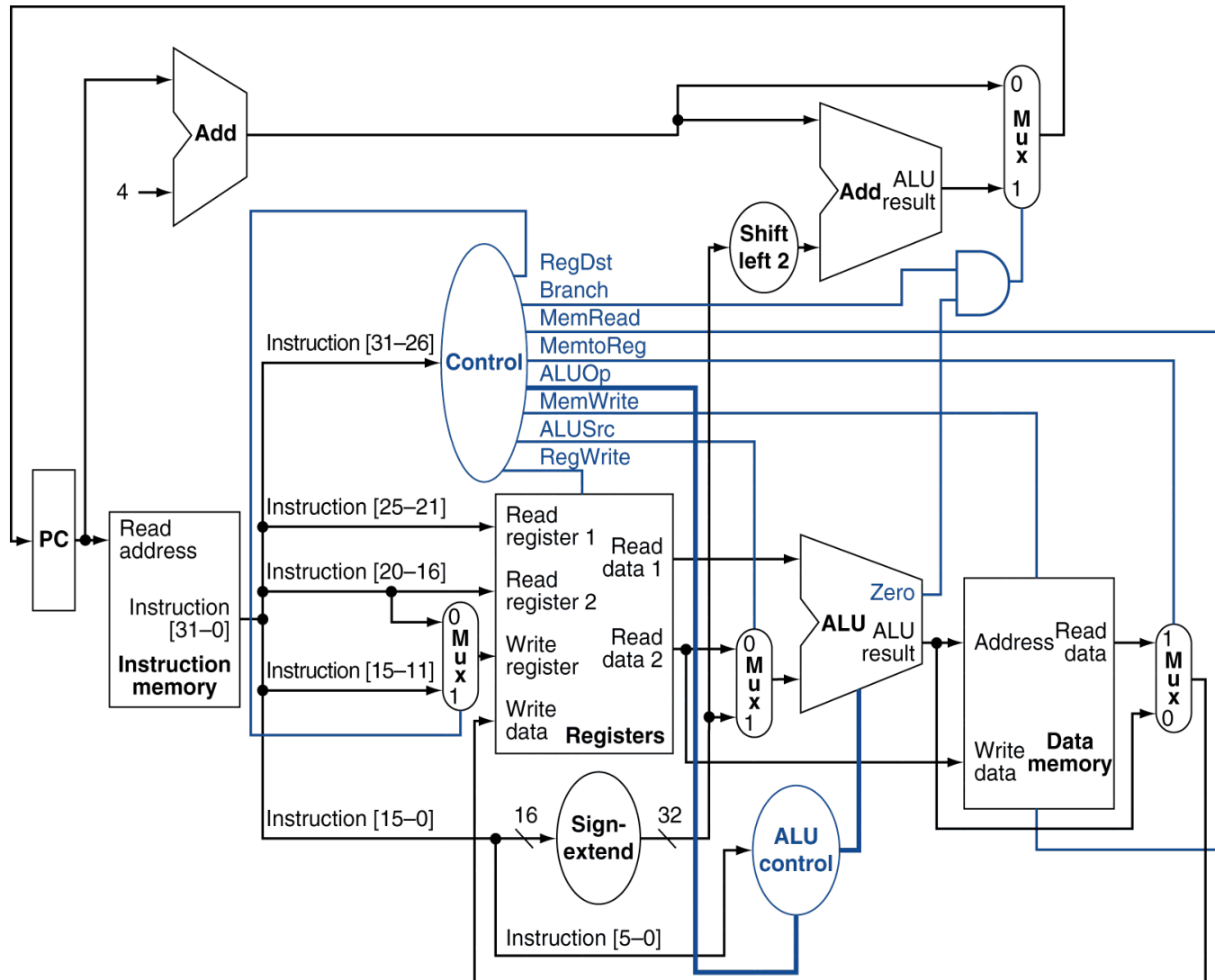
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- Consider the instruction sequence above:

Is there a data hazard assuming forwarding is used? If yes, by how many cycles?

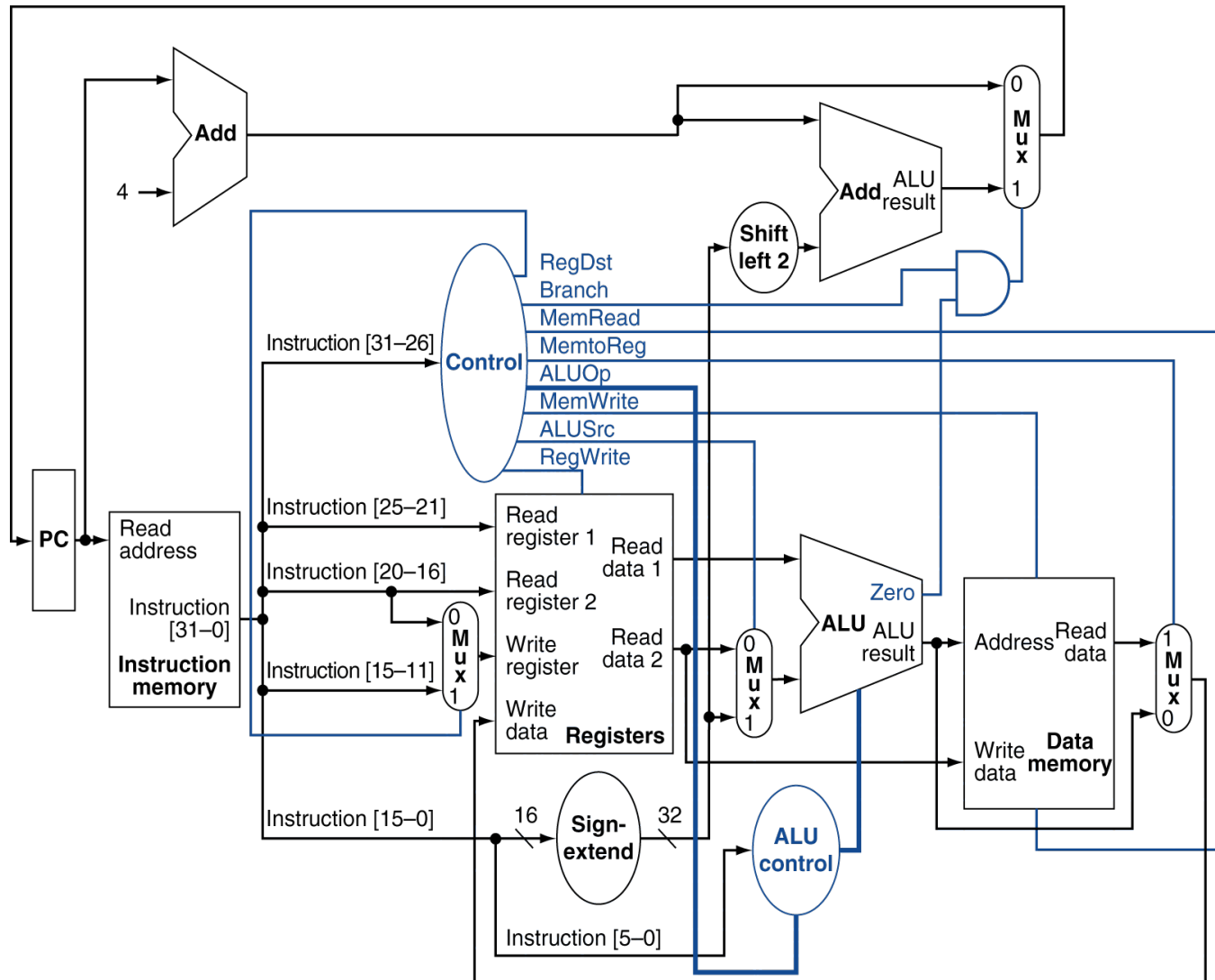
What is the value of RegDst for add \$t1,\$t2,\$t3?

Hint: destination address in bits 15-11.

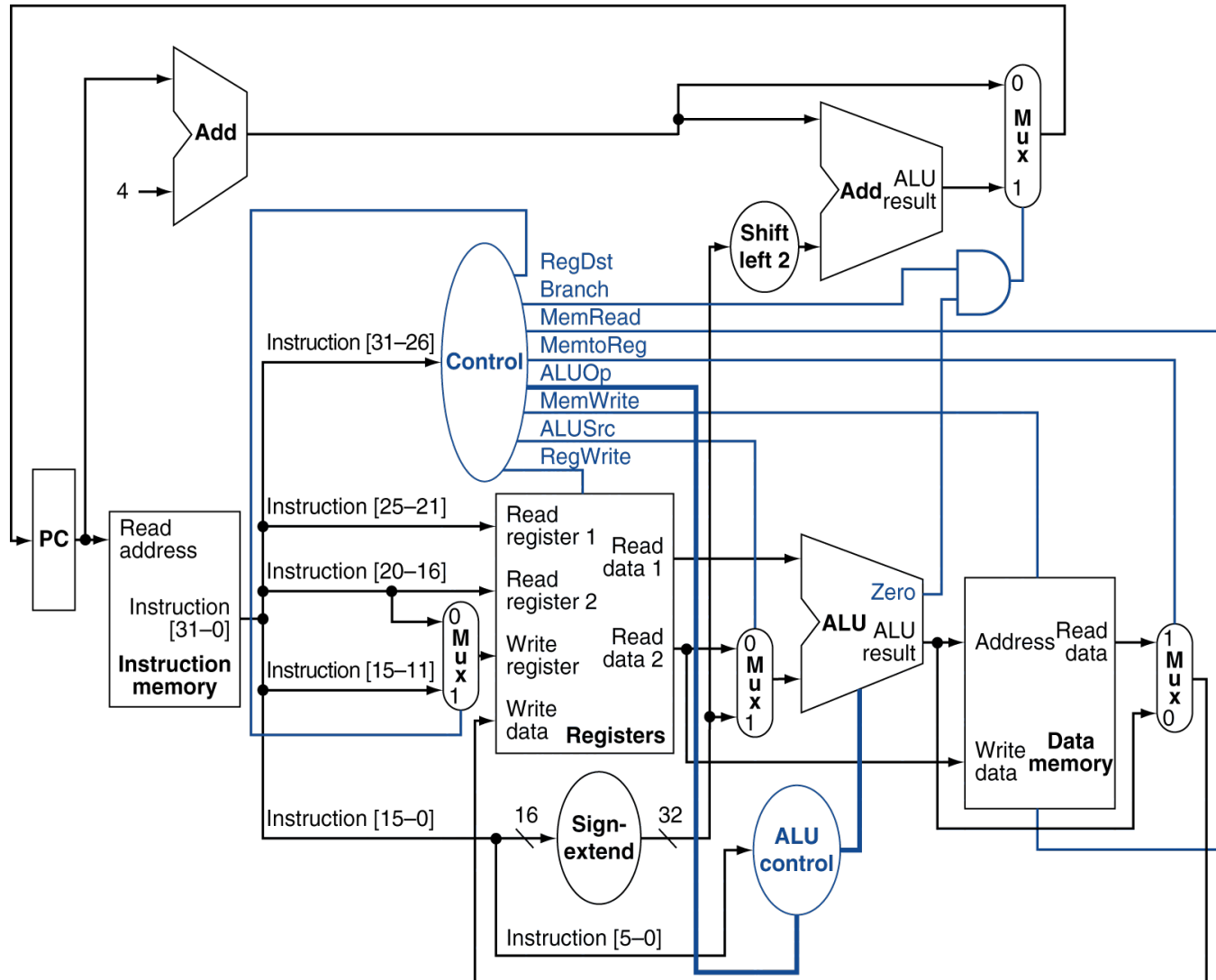




What is the value of ALUSrc for addi \$t1,\$t2,4?



What is the value of ALUSrc for lw \$t2,4(\$t3)?



What is the value of ALUSrc for beq \$t2,\$t3,exit?

