

CS 465- Fall 2017 Prof. Daniel A. Menasce Department of Computer Science













- Suppose that the above program runs on a machine that has a cycle time of 200 ps. What is the execution time of the program on this machine?
 - 1,650,000 cycles * 200 * 10⁻¹² = 3.3 * 10⁻⁴ sec = 0.33 msec



Suppose that compiler optimization is used to compile the same program as before. The optimization reduces the total number of instructions by 10% and now 12% of the instructions of the program take 2 cycles, 28% take 3 cycles, and 60% take 1 cycle. What is the execution time of the program now?

 -0.9 * 1,000,000 * (0.12 * 2 + 0.28 * 3 + 0.6 * 1) *

200 * 10⁻¹² = 3.024 * 10⁻⁴ sec



Answer

 Consider that 20% percent of a program's instructions are branch instructions and that the CPI for these instructions is 2. The CPI for the remaining instructions is 1.8. What would be the CPI of the program if the hardware designers improved the branch prediction algorithm so that the CPI of branch instructions went down to 1.2?

-0.2 * 1.2 + 0.8 * 1.8 = 1.68









 How would you compute the CPU time of a program as a function of the number of instructions, the CPI, and the clock cycle duration?

CPU time = # instructions * CPI * clock cycle duration

<section-header><section-header><section-header><section-header><text>









Answer

 What is the MIPS instruction needed to load element A[2] of array A into register \$t0 assuming the address of the array is stored at register \$s0 and that each element of the array is a 4-byte integer?

– lw \$t0, 8 (\$s0)







































Consider a 2 x 3 matrix stored in memory in *column major order*, i.e., elements are stored column by column. Each element is 4-bytes long. What is the byte offset of element i,j?

Byte offset of [i,j] =[j * 2 + i] * 4 because before [i,j] there are j full columns and i elements

2

Question Write a minimal set of MIPS assembly instructions that does the identical operation as the C code below. Assume the base address of C is in \$s1 and that A is in \$s2. Use the minimum number of registers. Do not destroy the contents of \$s1 or \$s2. A = C[0] << 4;

42

41

Write a minimal set of MIPS assembly instructions that does the identical operation as the C code below. Assume the base address of C is in \$s1 and that A is in \$s2. Use the minimum number of registers. Do not destroy the contents of \$s1 or \$s2.

A = C[0] << 4;

lw	\$t1, 0(\$s1)	# \$t1 <- C[0]
sll	\$t1, \$t1,4	# \$t1 <- \$t1 << 4
SW	\$t1, 0(\$s2)	# A <- \$t1

43







Answer

Describe what the following MIPS code does.

	addi	¢ c 2 ¢ 0 ¢ 0	# \$c2 - 0	
	auui	JSZ,JU,JU	# 352 = 0	
	addi	\$t1,\$0,\$0	# \$t1 = 0	
LOOP	lw	\$s1,0(\$s0)	# \$s1 = Mem[\$s0]	
	add	\$s2,\$s2,\$s1	# \$s2 = \$s2+Mem[\$s0]	
	addi	\$s0,\$s0,4	# \$s0 = \$s0 + 4	
	addi	\$t1,\$t1,1	# \$t1 = \$t1 + 1	
	slti	\$t2,\$t1,100	# \$t1 = 1 if \$t1 < 100; \$t1 = 0 otherwise	
	bne	\$t2,\$0,LOOP	# branch to LOOP if \$t2 ≠ 0 (\$t1 < 100)	
DONE:				
[
Code meaning: store in \$s2 the sum of all 100 words stored starting at address \$s0				



Consider a multiprocessor with p processors. Assume that 25% of the instructions of a program can be executed in parallel using all p processors. The remaining 75% of the instructions have to be executed sequentially. Assume that the time to execute the program sequentially (i.e., using only one processor) is Ts. Give an expression for S(p), the speedup obtained when using p processors.

S(p) = Ts / (0.75 Ts + 0.25 Ts/p) = 1 / (0.75 + 0.25/p)

 $\lim S(p)$ when $p \rightarrow \infty = 1/0.75 = 4/3 = 1.33$

49















