CS 465 – Fall 2018 – Homework 3
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Team Allowed: maximum of two per team. The members of a team must be from the **same** CS 465 section.

State clearly the team member names and GMU IDs as comments in each page of the submitted report.

Due date: November 15th, 2018 before 11:59pm.

IMPORTANT:

(1) Start to work on the homework early.
(2) If you plan to do the homework with a classmate, make a determination early if your teammate is responsive.
(3) The explanation for your answers is required. **You will not get credit without explanation.**
(4) Use a word processor to type your answers to part II and generate a pdf file from it.
(5) Do not share your solutions or partial solutions on Piazza or any other platforms (electronic or otherwise) before the deadline. This assignment is individual to a group. If you want to ask questions about your solution, please ask the TAs or me.
(6) Plagiarism is not permitted in any form. We enforce the university policy and honor code

Late submissions are not accepted.

Use a Word processor to type your answers and generate a PDF file to submit your homework.

How to submit: The submission will be made via a blackboard link available to you. You must submit a PDF file answering all questions. For team projects, only one member of the team should submit the PDF file and the other should submit a one-page PDF file stating the names of both members of the team. If you fail to submit the one-page PDF file you will not get any credit for the homework.

The PDF file name should follow the following convention:
"cs465_hw3_LastName1_LastName2"(for 2-member teams), or
"cs465_hw3_LastName1" (for 1-member teams).

Question 1 [25 points]: Consider the following snippet of MIPS code and answer the following questions:

```
sw      r16, 12(r6)
lw      r16, 8(r6)
add     r5,r1,r16
slt     r3,r5,r4
```

Consider the MIPS pipeline architecture we have been discussing in class and consider the following latencies for the 5 stages of the pipeline

IF	ID	EX	MEM	WB
100 ps	120 ps	150 ps	180 ps	100 ps

(a) What is the cycle duration? Explain why.

(a) Draw a diagram like the one at the bottom of slide 57 for the four instructions above. You should consider that there are no structural hazards and that data hazards are taken care of by stalling the processor. Indicate by a bubble each cycle in which the processor stalls. How long does it take to execute all four instructions?

(b) Consider now that forwarding can be used to mitigate data hazards. Draw a diagram like the one at the bottom of slide 57 for the four instructions above. Clearly indicate any forwardings that may be needed to mitigate processor stalling. You should consider that there are no structural hazards. Indicate by a bubble each cycle in which the processor stalls. How long does it take to execute all four instructions?

Question 2 [25 points]: Consider the MIPS code below and answer the following questions.

```
        addi    $t0,$zero,0
        addi    $t1,$zero,100
loop    beq     $t0,$t1,exit
        addi    $t2,$t0,10
        sw      $t2, 0($s0)
        addi    $s0,$s0,4
        addi    $t0,$t0,1
        j       loop
exit  -----
```

(a) How many times will the beq statement be executed?
(b) Assume that a static branch-not-taken prediction is used. What percentage of time will the prediction be correct?

(c) Assume that a static branch-taken prediction is used. What percentage of time will the prediction be correct?

Question 3 [25 pts]: Consider the MIPS code below and answer the following questions.

```
        addi    $t0,$zero,0
        addi    $t1,$zero,100
loop    addi    $t2,$t0,10
        sw      $t2, 0($s0)
        addi    $s0,$s0,4
        addi    $t0,$t0,1
        bne     $t0,$t1,loop
out:    -----
```

(a) How many times will the bne statement be executed?

(b) Assume that a static branch-not-taken prediction is used. What percentage of time will the prediction be correct?

(c) Assume that a static branch-taken prediction is used. What percentage of time will the prediction be correct?

Question 4 [25 pts]: Consider the following sequence of instructions and answer the questions below.

```
lw      $t1,0($s0)
add     $t2,$t3,$t4
sw      $t5,4($t0)
```

Complete the table below with the values that should be stored in the ID/EX, EX/MEM, and MEM/WB pipeline registers for each of the three instructions above. If any of the values is not relevant for the instruction indicate that with an * (i.e., a don't care).

	ID/EX	EX/MEM	MEM/WB
lw	ALUSrc= ALUOp= RegDst= Sign Extended= Instr(20-16)= MemWrite= MemRead= MemToReg= RegWrite =	MemWrite= MemRead= MemToReg= Instr(20-16)= RegWrite =	MemToReg= Instr(20-16)= RegWrite =
add	ALUSrc= ALUOp= RegDst= Sign Extended = Instr(15-11) = MemWrite= MemRead= MemToReg= RegWrite =	MemWrite= MemRead= MemToReg= Instr(15-11) = RegWrite =	MemToReg= Instr(15-11) = RegWrite =
sw	ALUSrc= ALUOp= RegDst= Sign Extended= Instr(20-16) = MemWrite= MemRead= MemToReg= RegWrite =	MemWrite= MemRead= MemToReg= Instr(20-16)= RegWrite =	MemToReg= RegWrite =