CS 465 – Computer Systems Architecture

Prof. Daniel Menasce; Fall 2021; Homework 3

Department of Computer Science

George Mason University

Team Allowed: maximum of two per team.

State clearly team member names and GMU IDs in each page of submitted report.

IMPORTANT:

1. Start to work on the homework early.
2. If you plan to do the homework with a classmate, make a determination early on that your teammate is responsive.
3. The explanation for your answers is required. **You will not get credit without explanation.**
4. Only one of the students in a team should submit the whole report and the other should just submit a one-page pdf with the names and G#’s of both students in the team.

Late submissions are not accepted.

Student name 1:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ G# 1: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Student name 2\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ G# 2: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Question 1 [40 points]:** Consider the execution of an R-type instruction and of a lw I-type instruction in the single-cycle data path discussed in class and shown below:



Enter 1, 0, or x (for don’t care) in the table below for the various outputs of the control unit.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction Type | RegWrite | RegDst | Branch | MemRead | MemtoReg | MemWrite | ALUSrc |
| R-type |  |  |  |  |  |  |  |
| I-type (just lw) |  |  |  |  |  |  |  |

**Question 2 [60 points]:** Consider the figure below and complete the values for the three tables below the figure for the lw $t1, 32($t2) instruction. Note that for this instruction, $t1 is register rt and $t2 is register rs. Consider that the control unit generates the following output signals: RegDst, MemRead, MemToReg, ALUOp, MemWrite, ALUSrc, and RegWrite. The value of ALUOp is 00 for add operations. Use an ‘X’ in a cell of a table when the cell is not present in a section (i.e., EX, M, or WB) of a pipeline register.



|  |
| --- |
| **ID/EX Pipeline Register** |
|  | RegDst | MemRead | MemToReg | ALUOp | MemWrite | ALUSrc | RegWrite |
| EX |  |  |  |  |  |  |  |
| M |  |  |  |  |  |  |  |
| WB |  |  |  |  |  |  |  |
| Rs |  |
| Rt |  |

|  |
| --- |
| **EX/MEM Pipeline Register** |
|  | RegDst | MemRead | MemToReg | ALUOp | MemWrite | ALUSrc | RegWrite |
| M |  |  |  |  |  |  |  |
| WB |  |  |  |  |  |  |  |
| Rt |  |

|  |  |  |  |
| --- | --- | --- | --- |
| **MEM/WB Pipeline Register** |

|  |  |
| --- | --- |
|  | 2 |

 |
|  | RegDst | MemRead | MemToReg | ALUOp | MemWrite | ALUSrc | RegWrite |
| WB |  |  |  |  |  |  |  |
| Rt |  |